

Roll No.

2415

B. E. 7th Sem. (CSE)

Examination – December, 2011

ADVANCED COMPUTER ARCHITECTURE

Paper : CSE-401 E

Time : Three hours]

[Maximum Marks : 100

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt any *five* questions. All questions carry equal marks.

1. (a) Explain the instruction set in detail. 14

(b) Explain how the virtual address converting into real address with a suitable example. 6

2. (a) Assume a wafer has diameter of 20 cm and cost \$ 4,000 for a particular production run. Compute the cost per die for die area = 2.3 cm^2 for 1 cm^2 if $\rho_D = 1 \text{ defect/cm}^2$. 10

- (b) Explain processor evaluation matrix with suitable example. 10

3. (a) Suppose we have the following parameters for an L1 cache with 4KB and an L2 cache with 64KB.

The cache miss rate is

4KB 0.10 misses per refr

64KB 0.20 misses per refr

1 REFR/I

3-CYCLES L1 miss, L2 hit

10 CYCLES total time L1 miss, L2 miss

What is the excess CPI due to cache misses ? 10

- (b) Explain the various techniques of cache organization in detail. 10

4. (a) Explain Hellermans and Raus model in detail. 10

- (b) Explain the open, closed, and mixed queue models in detail. 10

5. Explain synchronization and coherency. Also discuss memory coherence in shared memory multiprocessors. 20

6. (a) What is the use of micro program sequencer in micro programmed control unit ? Also describe the working of micro program sequencer. 10

(b) Explain the two level cache and write assembly cache in detail. 10

7. Assume we have a vector processor with the following parameters :

Processor cycles = 12ns

s, the number of simultaneously memory request per cycle = 3

$$T_c = 65\text{ns}$$

T, cycles per $T_c = 5$

M, modules = 17

Compute the worst case performance and relative performance. 20

8. Write short notes on the following :

20

(a) D-cache

(b) Selection of queuing model

(c) Vector processor

(d) T cycles in V-R translation

StudentSuvidha.com